REMARKS/ARGUMENTS

Claims 1-21 are pending in the application. Claims 1, 6, and 15-19 are amended herein. The Applicant hereby requests further examination and reconsideration of the application in view of the foregoing amendments and these remarks.

On page 2 of the office action, the Examiner rejected claims 1-3, 6, 8, 10, and 15-19 under 35 U.S.C. 102(e) as being anticipated by Nguyen. On page 5, the Examiner rejected claims 20-21 under 35 U.S.C. 103(a) as being unpatentable over Nguyen. On page 6, the Examiner objected to claims 4-5, 7, 9, and 11-14 as being dependent upon a rejected base claim, but indicated that those claims would be allowable if rewritten in independent form. For the following reasons, the Applicant submits that all of the pending claims are allowable over Nguyen.

Claims 1, 15, and 16

According to currently amended claim 1, the at least one programmable I/O buffer (PIB) can be programmed to support three or more of a double data rate (DDR) input mode, one or more demux input modes, one or more DDR demux input modes, and one or more additional input modes that do not involve any demultiplexing or DDR-to-SDR conversion, where the one or more demux input modes are different from the DDR input mode.

In addition, the at least one PIB can be programmed to support three or more of a DDR output mode, one or more mux output modes, one or more DDR mux output modes, and one or more additional output modes that do not involve any multiplexing or SDR-to-DDR conversion, where the one or more mux output modes are different from the DDR output mode.

Nguyen teaches a programmable I/O element that supports a DDR input mode (see column 8, lines 43-57) that is similar to the DDR input mode of claim 1. Nguyen also teaches a standard SDR input mode (see column 8, lines 15-42) that does not involve any demultiplexing or DDR-to-SDR conversion. As such, Nguyen's standard SDR input mode is an example of the one or more additional input modes of claim 1.

However, Nguyen does not teach the "one or more demux input modes" of claim 1 that are different from the DDR input mode. Nor does Nguyen teach the "one or more DDR demux input modes" of claim 1.

Similarly, Nguyen's programmable I/O element supports a DDR output mode (see column 8, lines 43-57) that is similar to the DDR output mode of claim 1. Nguyen also teaches a standard SDR output mode (see column 8, lines 15-42) that does not involve any multiplexing or SDR-to-DDR conversion. As such, Nguyen's standard SDR output mode is an example of the one or more additional output modes of claim 1.

However, Nguyen does not teach the "one or more mux output modes" of claim 1 that are different from the DDR output mode. Nor does Nguyen teach the "one or more DDR mux output modes" of claim 1.

Thus, while Nguyen may be said to teach a PIB that supports (1) two of the four types of input modes of claim 1 and (2) two of the four types of output modes of claim 1, Nguyen does not teach or even suggest a PIB that supports (1) at least three of the four types of input modes of claim 1 and (2) at least three of the four types of output modes of claim 1.

For all these reasons, the Applicant submits that claim 1 is allowable over Nguyen. For similar reasons, the Applicant submits that claims 15 and 16 are allowable over Nguyen. Since claims 2-14 depend variously from claim 1, it is further submitted that those claims are also allowable over Nguyen.

Claim 6

According to currently amended claim 6, the PIB supports a plurality of different demux input modes having different levels of demuxing, a plurality of different DDR demux input modes having different levels of demuxing, a plurality of different mux output modes having different levels of muxing, and a plurality of different DDR mux output modes having different levels of muxing. The only level of demuxing taught in Nguyen is 1:2 demuxing. Similarly, the only level of muxing taught in Nguyen is 2:1 muxing, As such, this provides additional reasons for the allowability of claim 6 over Nguyen.

Claim 17

Claim 17 has been amended to include the features of original claim 18. According to currently amended claim 17, the at least one PIB comprises a transfer stage adapted to apply a time-domain transfer to one or more data signals, wherein the transfer stage is adapted to be driven by a system clock signal corresponding to the time domain of the logic core.

In rejecting original claims 17 and 18, the Examiner cited multiplexer 330 as an example of the transfer stage of claim 17 and the clock clk of AND gate 335 as an example of the system clock signal of claim 18 that drives the transfer stage. Significantly, the Examiner provided absolutely no citation to any teaching in Nguyen for the feature explicitly recited in original claim 18 that the system clock signal is "corresponding to the time domain of the logic core."

The fact is that there is no teaching or even suggestion in Nguyen that the clock signal clk corresponds to the time domain of the logic core. Rather, Nguyen explicitly teaches that the clk signal "may be from the same source as the CLKOR signal," which is itself used to drive the rest of the circuitry in Nguyen's output block 300. See column 6, lines 25-28 and lines 43-63. There is no teaching or any suggestion anywhere in Nguyen that any of the clock signals used to drive any circuitry in the programmable I/O element corresponds to the time domain of Nguyen's logic core.

The Applicant submits therefore that currently amended claim 17 is allowable over Nguyen. Since claims 18-19 depend variously from claim 17, it is further submitted that those claims are also allowable over Nguyen.

Claim 18

According to currently amended claim 18, the transfer stage forms an interface between the logic core and additional circuitry within the at least one PIB. Support for this amendment is found, for example, in Figs. 3 and 5. As mentioned in the previous section, Nguyen cites multiplexer 330 as an example of the transfer stage. Significantly, as shown in Figs. 1 and 3, multiplexer 330 is internal to Nguyen's programmable I/O element and therefore does not form an interface between Nguyen's logic core and additional circuitry within the programmable I/O element. The Applicant submits that this provides additional reasons for the allowability of claim 18 over Nguyen.

Claim 19

According to currently amended claim 19, the additional circuitry within the at least one PIB is adapted to be driven by another clock signal not corresponding to the time domain of the logic core. Support for this amendment is found, for example, in Figs. 3 and 5, where SC corresponds to the time domain of the logic core and EC might not correspond to the time domain of the logic core. Nguyen does not teach such a combination of features as recited in currently amended claim 19. As such, the Applicant submits that this provides additional reasons for the allowability of claim 19 over Nguyen.

Claim 20

According to claim 20, the at least one PIB comprises DDR circuitry and demultiplexing circuitry, where the demultiplexing circuitry is programmable to demultiplex each of the two SDR data signals generated by the DDR circuitry into two or more lower-rate SDR data signals. As described earlier, Nguyen teaches a programmable I/O element having DDR circuitry, but Nguyen does not teach or even suggest a programmable I/O element that also has demultiplexing circuitry, let alone demultiplexing circuitry that can demultiplex the two SDR data signals generated by the DDR circuitry.

In rejecting claim 20, the Examiner admitted that Nguyen does not teach the claimed demultiplexing circuitry. Nevertheless, the Examiner stated that "it is well known in the art that logic blocks of the FPGA can be programmed to shift signals via demultiplexer into lower-rate signals."

First of all, the Examiner provides absolutely no support for his statement. Moreover, the Examiner refers to "logic blocks of the FPGA," while the present invention is directed to a programmable I/O buffer (PIB) that is part of the I/O interface of a programmable logic device (PLD) that is different from the logic core of the PLD. Thus, the PIB is not part of the PLD's logic core. Furthermore, even if it were true that "demultiplexing" per se is known, the fact remains that providing a PIB that can combine DDR-to-SDR conversion with demultiplexing is not known.

In view of the foregoing, the Applicant submits that claim 20 is allowable over Nguyen.

Claim 21

According to claim 21, the at least one PIB comprises DDR circuitry and multiplexing circuitry, where the multiplexing circuitry is programmable to multiplex four or more outgoing SDR data signals into two higher-rate SDR data signals, where the two higher-rate SDR data signals are converted into an outgoing DDR data signal by the DDR circuitry. As described earlier, Nguyen teaches a programmable I/O element having DDR circuitry, but Nguyen does not teach or even suggest a programmable I/O element that also has multiplexing circuitry, let alone multiplexing circuitry that can multiplex four or more SDR data signals into two higher-rate SDR data signals for application to the DDR circuitry.

In rejecting claim 21, the Examiner admitted that Nguyen does not teach the claimed multiplexing circuitry. Nevertheless, the Examiner stated that "it is well known in the art that logic blocks of the FPGA can be programmed ... to shift signals via multiplexer into higher-rate signals."

First of all, the Examiner provides absolutely no support for his statement. Moreover, the Examiner refers to "logic blocks of the FPGA," while the present invention is directed to a programmable I/O buffer (PIB) that is part of the I/O interface of a programmable logic device (PLD) that is different from the logic core of the PLD. Thus, the PIB is not part of the PLD's logic core. Furthermore, even if it

were true that "multiplexing" per se is known, the fact remains that providing a PIB that can combine multiplexing with SDR-to-DDR conversion is not known.

In view of the foregoing, the Applicant submits that claim 21 is allowable over Nguyen.

In view of the foregoing, the Applicant submits therefore that the rejections of claims under Sections 102(e) and 103(a) have been overcome.

In view of the above amendments and remarks, the Applicant believes that the pending claims are in condition for allowance. Therefore, the Applicant believes that the entire application is now in condition for allowance, and early and favorable action is respectfully solicited.

Respectfully submitted,

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